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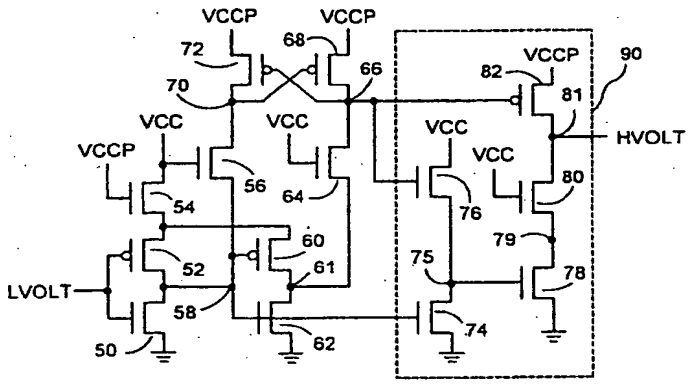
(54) Low-to-high voltage translator with latch-up immunity.

(57) A fast low-to-high voltage translator with immunity to latch-up. The circuit includes a voltage comparator and employs at least one transistor (52, 60) which is used to quickly pull up a node. It further uses another transistor (54) which is capable of limiting the voltage at certain nodes (58, 66, 70) in order to eliminate latch-up if a pumped power supply is provided to the circuit. Latch-up therefore is eliminated during power-up. Other transistors (56, 64) are utilized as voltage drop limiters to limit the voltage drop across other transistors during switching. This provides improved reliability by reducing substrate current and hot carriers.

FIG. 3



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The further object of the present invention is to minimize current flow from a power supply providing VCCP to another potential, such as ground.

The present invention provides a fast low-to-high voltage translator with latch-up immunity. The circuit includes a voltage comparator which compares an input voltage to its complement. It is coupled to receive a low power supply (VCC) and a high power supply (VCCP). The high voltage supply (VCCP) may be a pumped power supply. The output of this circuit may be buffered to provide logic functions, and to drive large loads.

A novel and important aspect of the present invention is that it provides high-speed switching with latch-up immunity when implemented with a pumped power supply.

A salutary aspect of the present invention is that it minimizes the current between the high voltage supply and ground.

The invention, together with its objects and the advantages thereof, may best be understood by reference to the following detailed description taken in conjunction with the accompanying drawings, of which:

Fig. 1 is a detailed diagram of a prior art circuit that translates a low voltage to a high voltage.

Fig. 2 is schematic diagram of a first embodiment of the present invention.

Fig. 3 shows a second embodiment of the present invention.

Fig. 4 shows a third embodiment of the present invention.

Figs. 5(a) and (b) are modifications of the Fig. 3 embodiment.

Fig. 6 is a modification of the Fig. 4 embodiment.

Fig. 2 illustrates an improvement over the Fig. 1 circuit. Like devices and nodes of Figs. 1 and 2 will be designated with the same numbers. Nodes 30 and 32 are coupled to VCC through source-drain paths of transistors 40 and 42, respectively. Transistors 12 and 14 have been eliminated. The gate electrodes of transistors 16 and 42 are directly coupled to node 30. The gate electrodes of transistors 10 and 40 are coupled to receive signal LVOLT.

Transistors 10 and 40 form a first inverter, and transistors 16 and 42 form a second inverter. Each inverter is coupled between VCC and ground (0V). Whatever the voltage of an input signal LVOLT, the inverted or opposite voltage will be provided on node 30 by transistors 10 and 40. The voltage at node 32 will be provided by transistors 16 and 42 as the same voltage as signal LVOLT.

When the voltage of signal LVOLT is VCC, the respective voltages at nodes 30 and 32 are 0V and VCC. Node 26 is clamped to 0V through turned-on transistor 28. Node 18 is pulled to VCC-Vt_N through turned-on transistor 20. Node 26 supplies 0V to the gate electrode of transistor 24 to turn it on harder (the gate-source voltage is more negative than a threshold voltage Vt_P). This pulls node 18 to VCCP and turns off transistor 20.

Node 18 first provides VCC - Vt_N to the gate electrode of transistor 22 to decrease its current drive capability and then provides VCCP to the gate electrode of transistor 22 to turn it off completely. Node 26 is pulled further to 0V. Output signal HVOLT supplied by node 18 is approximately VCCP.

When the voltage of signal LVOLT is 0V, the respective voltages at nodes 30 and 32 are VCC and 0V. Node 18 is clamped to 0V through turned-on transistor 20. Node 26 is pulled to VCC-Vt_N through turned-on transistor 28. When the voltage at node 26 rises to VCC- Vt_N transistor 28 will turn off. Node 18 supplies 0V to the gate electrode of transistor 22 to turn it on harder (the gate-source voltage is more negative than a threshold voltage Vt_P). This pulls node 26 to VCCP.

Node 26 first provides VCC - Vt_N to the gate electrode of transistor 24 to decrease its current drive capability and then provides VCCP to turn off transistor 24 completely. Node 18 is then pulled closer to 0V. Output signal HVOLT is supplied by node 18 and has a voltage of approximately 0V.

Transistors 20 and 28 are used to limit the drain-to-source voltages across transistors 16 and 10, respectively, to VCC - Vt_N during switching. For example, if transistor 22 is on (the gate-source voltage of transistor 22 is more negative than or equal to Vt_P), the voltage at node 26 is VCCP. If transistor 28 is eliminated and transistor 10 is on (the voltage of signal LVOLT is high at the gate electrode of transistor 10), there would be a voltage drop across transistor 10 equal to VCCP - VSS (>VCC). This voltage drop may cause substrate current and hot carriers if the device has small dimensions which may permanently damage the transistor.

Transistors 20 and 28 also eliminate the latch-up of transistors 42 and 40, respectively. For example, if transistor 22 is on (the gate-source voltage of transistor 22 is more negative than or equal to Vt_P), the voltage at node 26 is VCCP. If transistor 28 were eliminated, the voltage at the drain electrode of transistor 40 would be VCCP. If the substrate of transistor 40 were coupled to receive VCC, then the drain-substrate region of transistor 40 would be forward biased. The forward bias may cause transistor 40 to latch-up.

output signal HVOLT. Typically, VCCP ≈ 5V, VCC ≈ 3V and VSS (ground) ≈ 0V.

The circuit defined by a block 90 (circuit elements 74 to 82) in Fig. 3 represents a buffered output stage. The purpose of buffered output stage 90 is to drive large capacitive loads. It can be configured to so that signal HVOLT either follows or is the complement of signal LVOLT.

Transistors 72, 68 and 82 are p-channel and have their bodies coupled to the third power supply providing VCCP. Transistors 52 and 60 also are p-channel, but have their bodies coupled to the first power supply providing VCC.

Transistors 56, 64 and 80 are used to limit the drain-to-source voltages across transistors 50, 62 and 78, respectively, to VCC - Vt_N during switching. For example, if transistor 72 is on (the gate-source voltage of transistor 72 is less than or equal to Vt_P), the voltage at node 70 is VCCP. If transistor 56 were eliminated and transistor 50 is on (from LVOLT being high at the gate electrode of transistor 50), there would be a voltage drop across transistor 50 equal to VCCP - VSS (>VCC). This voltage drop may cause substrate current and hot carriers if the device were to have small dimensions.

Transistors 56 and 64 also function to limit the drain-substrate voltage (i.e. PN junction voltage) of transistors 52 and 60. In the instance where the voltage at node 58 is allowed to increase to VCCP (transistor 56 is eliminated), the drain-substrate voltage drop would be VCCP - VCC. This voltage drop is greater than a drain-substrate junction voltage VD. Therefore, the drain-substrate junction will be forward biased and current will be caused to flow into the substrate. As a result, transistor 52 will probably latch-up.

The addition of transistor 56 decreases the voltage drop across turned-on transistor 50. If the voltage at node 70 is VCCP, and the voltage at the gate electrode of transistor 56 is VCC (VCCP ≥ VCC), then transistor 56 will only pull node 58 to VCC - Vt_N. Transistor 56 will turn off if the voltage at node 58 rises past VCC - Vt_N (<VCCP).

To summarize, the inclusion of transistors 56 and 64 will eliminate the problems mentioned supra. For example, transistor 56 will pass a voltage VCCP up to a maximum of VCC - Vt_N during power-up. Therefore, the drain-substrate region of transistor 52 will not forward bias, even during normal operation, regardless of what voltage the substrate is biased to.

Transistors 52 and 60 are implemented to speed up the operation of this preferred embodiment by coupling nodes 58 and 61 to VCC. However, transistor 54 is added to avoid latch-up during power-up of the circuit by preventing nodes 66 and 70 from rising above VCCP - Vt_N. Similar to the explanation of Fig. 2, if the source electrode of transistor 52 were coupled directly to receive VCC (transistor 54 removed), then on power-up the voltage at node 58 would be VCC if signal LVOLT were low (0V). Turned-on transistor 56 will couple node 70 to VCC - Vt_N.Node 70 cannot rise to a greater voltage because transistor 56 will turn off. If the voltage at node 70 were a diode voltage VD greater than VCCP, the PN drain region may forward bias which would inject current into the substrate. This may cause latch-up.

By adding transistor 54 to the Fig. 3 embodiment (as illustrated), the voltage at the source electrode will be regulated to VCCP - Vt_N until VCCP is a threshold greater than VCC. At that point, the source electrode will not increase past VCC. Thus the voltage at node 58 will be VCCP - Vt_N up to a maximum of VCC. Transistor 56 will clamp node 70 (transistor 72 is off) to a maximum of VCC - Vt_N.Node 70 cannot rise above VCC - Vt_N since transistor 56 will turn off. The voltage at node 70 will be VCCP - Vt_N up to a maximum of VCC - Vt_N. The drain-substrate voltage will not forward bias the drain-source region. Transistor 72 will not latch-up.

The function of transistor 54 will be explained by way of an example. During power-up, VCCP = 2V, VCC = 3V, Vt_N = 1V, VD = 0.5V, and LVOLT = 0V. The voltage at the source electrode of transistor 54 equals VCCP - Vt_N = 1V. Since transistor 52 is turned on by signal LVOLT (0V), the voltage at node 58 equals 1V. VCC at the gate electrode of transistor 56 allows node 70 to be clamped to 1V. Since the PN drain region has a voltage from the drain electrode to the substrate of 1V - 2V = -1V (<VD), the PN drain region is not forward biased. No latch-up occurs.

As another example, consider these conditions: VCCP = 5V, VCC = 3V, Vt_N = 1V, VD = 0.5V, and LVOLT = 0V. The voltage at the gate electrode of transistor 54 is greater than a threshold voltage Vt_N above VCC. Therefore, the full voltage VCC at the drain electrode of transistor 54 will be passed to the source electrode of transistor 54. Signal LVOLT turns turned-on transistor 52 to clamp node 58 to VCC. Transistor 56 will clamp node 70 only to VCC - Vt_N since the voltage at the gate electrode of transistor 56 is VCC. Since the PN drain region has a voltage from the drain electrode to the substrate of VCC - VCCP = -2V (<VD), the PN drain region is not forward biased. No latch-up occurs.

Transistors 76 and 74 comprise a push-pull stage which prevents crowbar current from passing from VCCP to VSS of the buffered output stage. "Crowbar" current is current from a high voltage supply to a low voltage supply during device switching. Transistor 74 is larger than transistor 76 so that node 75 is pulled low before node 66 is pulled low, thereby turning off transistor 78 before transistor 82 turns on. This

Node 104 from the first inverter is coupled to a source electrode of a transistor 116. A gate electrode of transistor 116 is coupled to node 114. A drain electrode of transistor 116 is coupled to a node 118. Node 118 is coupled to a drain electrode of a p-channel transistor 120. A gate electrode of a transistor 120 is coupled to a node 122. A source electrode of transistor 120 is coupled to receive VCCP, which is also coupled to the body of transistor 120.

Node 118 is coupled to a gate electrode of a p-channel transistor 124. A source electrode of transistor 124 is coupled to receive VCCP. A drain electrode of transistor 124 is coupled to node 122. Node 122 is coupled to a drain electrode of a transistor 126. A gate electrode of a transistor 126 is coupled to node 104. A source electrode of a transistor 126 is coupled to node 114.

Node 114 is coupled to gate electrodes of a third inverter between node 108 and ground. The third inverter comprises transistors 128 and 130 having an output node 132. A source electrode of transistor 128 is coupled to ground. Drain electrodes of transistors 128 and 130 are coupled together. A source electrode of transistor 130 is coupled to node 108. Drain electrodes of transistors 128 and 130 are coupled to a source electrode of a transistor 132. A gate electrode of transistor 132 is coupled to node 114. A drain electrode of transistor 132 is coupled to a node 134.

Node 134 is coupled to a drain electrode of a transistor 136. A gate electrode of transistor 136 is coupled to node 122. A source electrode of transistor 136 is coupled to receive VCCP. A signal HVOLT is provided at node 134.

The circuit defined by a block 140 (elements 128 to 136) in Fig. 4 represents a buffered output stage. The purpose of the buffered output stage is to drive large capacitive loads. It can be configured to so that signal HVOLT either follows or is the complement of signal LVOLT.

Transistors 116, 126 and 132 serve the same functions as transistors 56, 64 and 80 of Fig. 3. Additionally, their respective gate electrodes are not connected to VCC, but are connected to active nodes within the Fig. 4 embodiment. This configuration is done to increase the switching speed and to reduce crowbar current (explained *infra*).

P-channel transistors 120, 124 and 136 have their bodies coupled to the third power supply providing VCCP. Transistors 102, 112 and 130 have their bodies coupled to the first power supply providing VCC.

The operation of the Fig. 4 embodiment will now be explained. When the input signal LVOLT is VCC, transistor 100 is turned on to clamp node 104 to 0V. Transistor 102 is turned off. With VCCP being applied to the gate electrode of transistor 106 to maintain it on, node 108 is clamped to VCC since transistor 102 is off.

With 0V at node 104, transistor 110 turns off and transistor 112 turns on to clamp node 114 to VCC. Therefore, the voltage at node 114 is the inverse or complement of the voltage at node 104. VCC at node 114 and 0V at node 104 are respectively applied to the gate and source electrodes of transistor 116. Transistor 116 is turned on since the gate-source voltage is greater than a threshold voltage Vt_N. Turned-on transistor 116 pulls the voltage at node 118 to 0V (assuming transistor 120 is off).

VCC at node 114 and 0V at node 104 are respectively applied to the source and gate electrodes of n-channel transistor 126. Transistor 126 is turned off since the gate-source voltage is less than a threshold voltage Vt_N. Hence, node 122 is decoupled from node 114.

0V at node 118 is applied to the gate electrode of transistor 124. The gate-source voltage of transistor 124 (0V - VCCP) causes transistor 124 to turn on. The voltage at node 122 is clamped to VCCP since node 122 is not coupled to any other node. VCCP at node 122 is applied to the gate electrode of transistor 120. Transistor 120 is turned off because the gate-source voltage (VCCP - VCCP) is less negative than one threshold voltage Vt_P. Accordingly, node 118 is coupled to ground via the source-drain path of transistor 100, and neither transistor 102 nor 120 pull voltage up.

VCCP at node 122 is applied to the gate electrode of transistor 136. Since the gate-source voltage of transistor 136 (VCCP - VCCP) is less negative than a threshold voltage Vt_P, transistor 136 is turned off to isolate node 134 from VCCP.

VCC at node 114 turns turned-on transistor 128 and turns off transistor 130. Turned-on transistor 128 clamps the voltage at the source electrode of transistor 132 to 0V. With VCC at node 114 being applied to the gate electrode of transistor 132, transistor 132 is turned on to clamp the voltage at node 134 to 0V. Hence, signal HVOLT is 0V.

When signal LVOLT is 0V, transistor 100 is turned off, thereby to decouple node 104 from ground. Transistor 102 is turned on. Node 108 is coupled to VCC for reasons explained *supra* (VCCP at gate electrode of transistor 106 maintains it on; drain coupled to VCC). Thus, node 108 is clamped to VCC since transistor 100 is off. Further, turned-on transistor 102 clamps the voltage at node 104 to the voltage at node 108 (VCC).

channel transistor 49 can be coupled in series with transistor 50 between node 58 and ground as illustrated in Fig. 5 (a). Another input signal LVOLT2 is coupled to both gate electrodes of the additional p- and n-channel transistors as shown in Fig. 5 (a). This configuration would provide a logic AND function at node 66 and a logic NAND function as the output signal HVOLT. Table 1 shows the input-output characteristics of Fig. 5 (a).

TABLE 1

FIG. 5 (a) AND/NAND GATE			
LVOLT	LVOLT2	NODE 66	HVOLT
0V	0V	0V	VCCP
0V	VCC	0V	VCCP
VCC	0V	0V	VCCP
VCC	VCC	VCCP	0V

Referring to Fig. 5 (b), a source-drain path of a p-channel transistor 55 can be coupled in series with transistor 52 between node 58 and the source electrode of transistor 54. A source-drain path of an n-channel transistor 53 can be coupled in parallel with transistor 50 between node 58 and ground. Another input signal is coupled to both gate electrodes of the additional p- and n-channel transistors as shown in Fig. 5 (b). Table 2 shows the input-output characteristics of Fig. 5(b).

TABLE 2

FIG. 5 (b) OR/NOR GATE			
LVOLT	LVOLT2	NODE 66	HVOLT
0V	0V	0V	VCCP
0V	VCC	VCCP	0V
VCC	0V	VCCP	0V
VCC	VCC	VCCP	0V

Fig. 6 illustrates a modification of the Fig. 4 embodiment. Devices that are the same in Figs. 4 and 6 are designated by the same reference numerals. In Fig. 6, transistor 135 has its gate electrode coupled to another input signal X generated by other circuitry (not shown). A drain electrode of a further transistor 137 is coupled to node 134. A gate electrode is coupled to another input signal Y that is generated by other circuitry (not shown). A source electrode of transistor 137 is coupled to receive VCCP. Signals X and Y may be the identical signal, or they be time delayed relatives of one another, but at some time they preferably have the same logical signal state. However, the range of signal X is 0V to VCC while the range of signal Y is 0V to VCCP.

Fig. 6 is configured to output the logical NAND with respect to signals X and Y, and the voltage at node 114. For example, if the voltage at node 114 is VCC, the voltage of signal X is VCC, and the voltage of signal Y is VCCP, then transistor 128 is turned on and transistor 130 is turned off. Turned-on transistor 128 pulls the source electrode of transistor 135 to 0V. The voltage at node 122 is VCCP which will turn off transistor 136 to unclamp node 134 from VCCP.

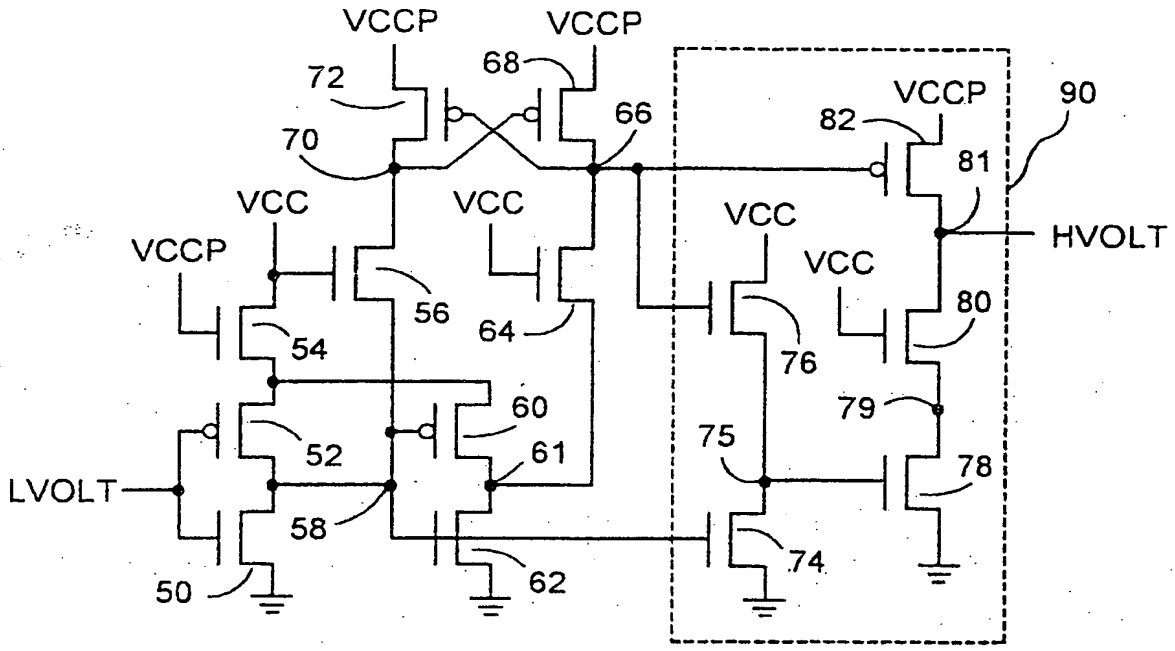
Signal X is VCC to turn-on transistor 135 to couple node 134 to the source electrode of transistor 135, which is coupled to ground (0V) through on transistor 128. Signal Y is at VCCP which turns off transistor 137 to uncoupled node 134 from VCCP. Therefore, the voltage at node 134 is clamped to 0V. See Table 3 for the input/output characteristics of Fig. 6.

10. The circuit of any preceding claim further characterized by a buffered output stage coupled to at least said output terminal, said buffered output stage configured to receive at least another signal (X, Y) to provide a logic AND function.

11. A method of operating a voltage translator circuit characterized by the steps of generating a first voltage at a first node (30, 58, 104) including selectively coupling the first node to first and second power supplies in response to an input signal (LVOLT), generating a second voltage at a second node (26, 70, 118) including selectively coupling the second node (32, 61, 114) to first and second power supplies in response to the input signal (LVOLT), and generating an output signal (HVOLT) in response to the input signal (LVOLT).

12. A method according to Claim 11 further characterized by the step of limiting at least a third node (26, 70, 118) voltage in response to a third voltage (VCCP).

FIG. 3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LVOLT
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FIG. 4

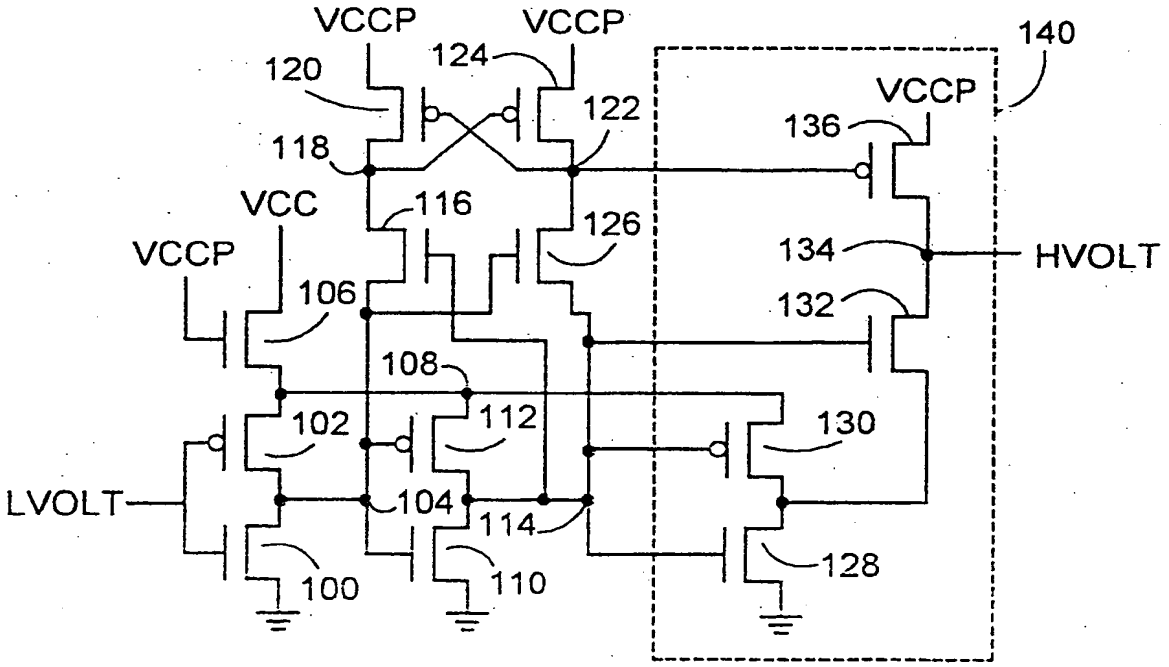
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FIG. 6

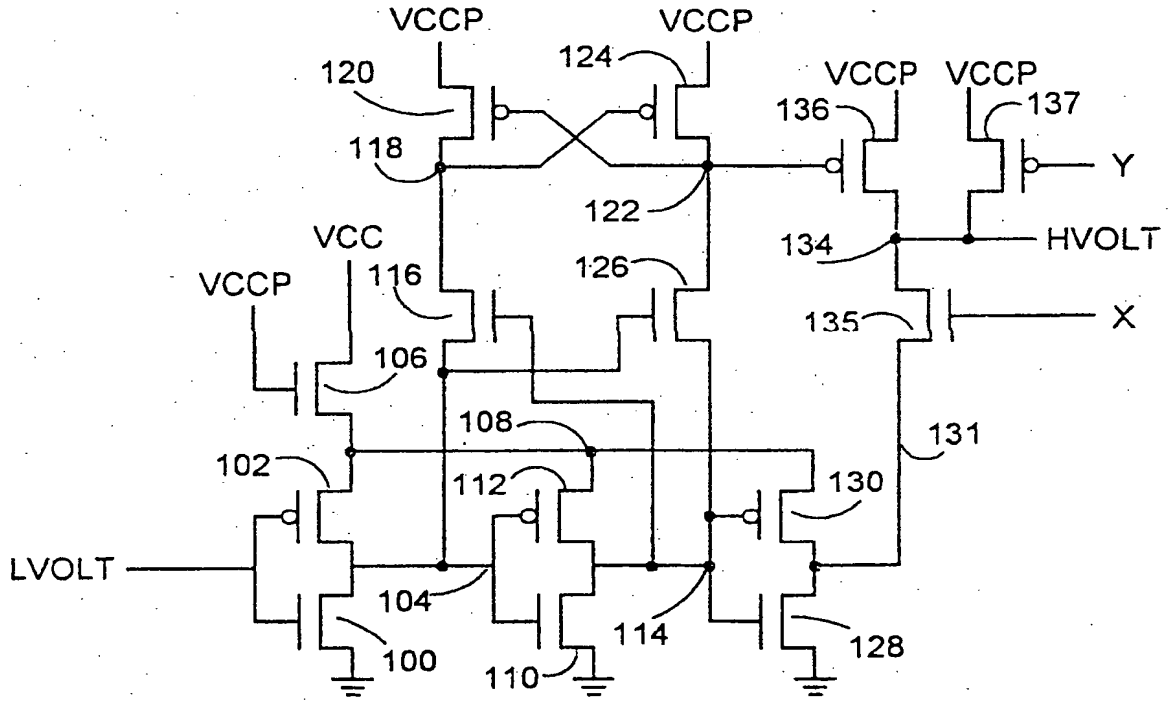
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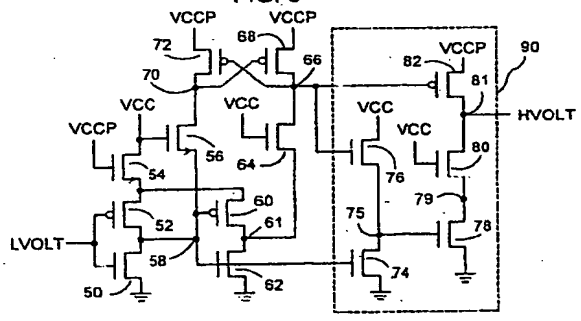
FIG. 3



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